RH1782 Product Datasheet

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Revision History

Rev	Date	Description
A	10/23/2024	Initial introduction

1 General Description

The RH1782 is a fault protected RS-485/RS-422 low-power transceiver that is in compliance with ANSI TIA/EIA485-A with a 5V supply, and operates with a 3.3V supply with reduced driver output voltage for low power applications. It contains one driver and one receiver configured internally into a bus port for half-duplex communication.

The RH1782 features a balanced fast driver that allows error-free data transmission up to 10Mbps.The receiver inputs have a failsafe feature that guarantee a logic-high output if the inputs are shorted or left opened, and each receiver supports up to 256 nodes on the network. In addition, the receiver has wide common-mode voltage range up to ±40V for multipoint applications over long cables.

This transceiver integrates many protections such as thermal shutdown, current-limiting, bus fault protection up to ±70V, and failsafe when the supply is under-voltage. It also provides robust ±30kV HBM protection, ±8kV IEC Contact, and ±15kV IEC Air Gap on bus pins. In addition, all pins can tolerate ±1.5kV CDM, and ±400mA Latch-up test.

The RH1782 is available in 8-pin SO package and operates over -40ºC to +125ºC extended temperature range.

2 Features

- ANSI TIA/EIA485-A, TIA/EIA422-B compliant
- Bus fault voltage protection to ±70V
- Operation with 3.3V to 5V supply range
- Low electromagnetic emission, and high electromagnetic immunity
- ±30kV HBM ESD tolerance on bus pins
- ±8kV IEC Contact Discharge and ±15kV IEC Air Gap Discharge
- All pins pass ±1.5kV CDM, and ±400mA Latch-up test
- Symmetrical transceiver propagation delays enhanced timing margin and symmetry
- Receiver extended common mode input voltage range from -40V to +40V
- 1/8 Unit Load for up to 256 nodes on one network
- Failsafe receiver for open-circuit, short-circuit, and idle bus conditions
- Data transmission rates up to 10Mbps
- Protection features: thermal-shutdown, under-voltage lockout, short-circuit current limit
- Available in industry-standard 8-pin SOIC package

3 Applications

- Low-power RS-485/RS-422 Transceivers
- Voltage Level translators
- Transceivers for EMI-sensitive applications
- HVAC networks, security electronics, building automation
- Industrial control and networks
- Telecommunication equipment, motion control
- Consumer applications
- Energy Storage Systems

4 Typical Operating Circuit

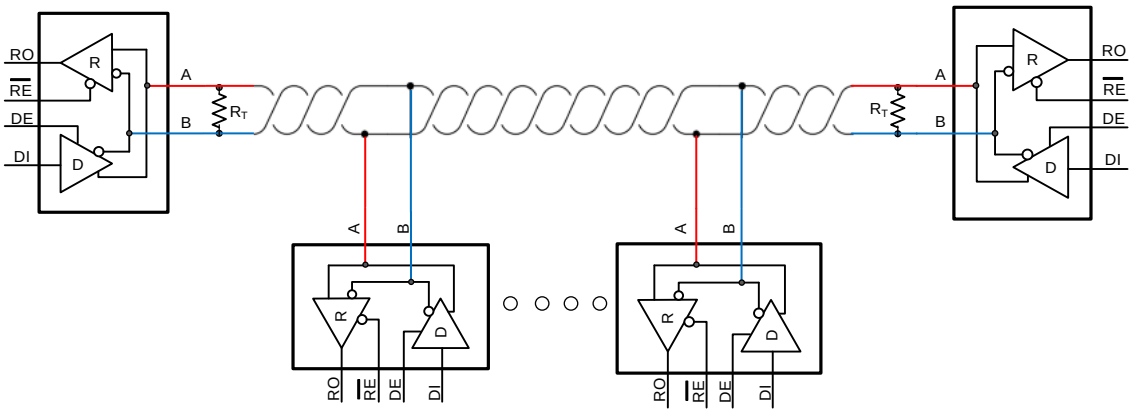
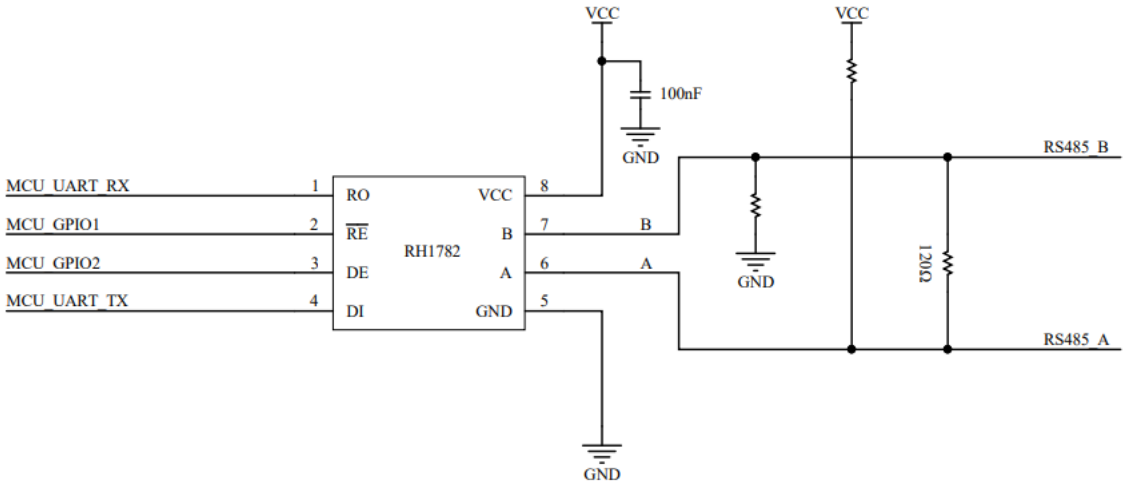


Figure 1 – Typical RS-485 Network Operating Circuit

Typical Application Circuit



5 Ordering Information

Part Number	Temperature Range	Package-Pin	Description
RH1782ASCE+	-40ºC to +125ºC	SO-8	Small outline 8-leads package, body width 3.9mm
RH1782ASCE+T	-40ºC to +125ºC	SO-8	SO-8, body width 3.9mm in tape and reel

Table 1 – Ordering Information

6 Pin Configuration and Functions

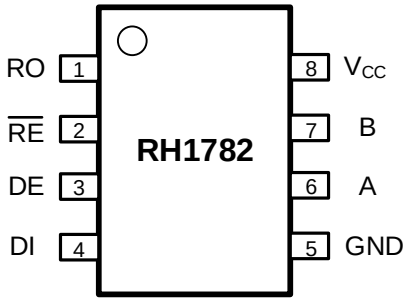


Figure 2 – Device in SO-8 Package

Pin Number	Pin Name	Pin Type	Description
1	RO	Digital Output	Receiver Data Output
2	$\overline{RE}$	Digital Input	Receiver Data Enable. Receiver is enabled when $\overline{RE}$ is at logic Low. Receiver is disabled to high impedance when RE is at logic High.
3	DE	Digital Input	Driver Enable. Driver outputs A and B are enabled when DE is at logic High. A and B are disabled to high impedance when DE is at logic Low.
4	DI	Digital Input	Driver Data Input
5	GND	Ground	Ground
6	A	Analog Bus I/O	Non-inverting Driver Output and Non-inverting Receiver Input
7	B	Analog Bus I/O	Inverting Driver Output and Inverting Receiver Input
8	VCC	Power	Power Supply

Table 2 – Pin Functions

7 Functional Description

The RH1782 is a RS-485/RS-422 half-duplex transceiver with individual Driver enable and Receiver enable pins. It has enhanced EMC and ESD protection for both digital and bus pins, bus fault voltage protection up to ±70V, an extended receiver input common-mode voltage range to ±40V, and failsafe features that provide ample application flexibility.

7.1 Operating modes

The RH1782 has individual enable pins for its driver and receiver through DE and $\overline{RE}$ pins.

Operating Mode	Transceiver status		Digital Input pins			Bus pins		Digital Output pin
	Driver	Receiver	DE	$\overline{RE}$	DI	A	B	RO
transmitting	enabled	disabled	High	High	Low	Low	High	high impedance
					High	High	Low	high impedance
receiving	disabled	enabled	Low	Low	X, don't care	A-B ≥ +0.2		High
						A-B ≤ -0.2		Low
						A & B left open		High
						A & B shorted		High
half-duplex, loopback	enabled	enabled	High	Low	Low	Low	High	Low
					High	High	Low	High
shut-down	disabled	disabled	Low	High	X, don't care	high impedance	high impedance	high impedance

Table 3 – Device Operating Modes

7.1.1 Transmitting mode

Connect DE to logic High and $\overline{RE}$ to logic High sets RH1782 to data transmitting mode. In this mode, the driver is enabled and the receiver is disabled. The driver transmits data through DI and outputs RS-485/RS-422 compliant signals at bus outputs A and B. When DI is at logic Low, bus pin A is sinking current from the load and bus pin B is sourcing current to the load; when DI is at logic High, bus pin A is sourcing current to the load and bus pin B is sinking current from the load. The driver can achieve data transmission rate up to 10Mbps.

7.1.2 Receiving mode

Connect DE to logic Low and $\overline{RE}$ to logic Low sets RH1782 to data receiving mode. In this mode, the driver is disabled and the receiver is enabled. Regardless to the logic state at DI, the driver is disabled and the driver outputs are in high impedance state, which allow pins A and B be driven from the bus. When bus pins A and B are driven differentially such that $V_A - V_B \geq +0.2V$, receiver output RO outputs a logic High; when bus pins A and B are driven differentially such that $V_A - V_B \leq -0.2V$, receiver output RO outputs a logic Low.

The RH1782 provides an internal biasing of the receiver input thresholds of ~ -100mV, such that the receiver output remains at logic High under open bus (both A & B are left open), and bus-short (both A and B are shorted together) conditions.

7.1.3 Half-duplex/loopback mode

Connect DE to logic High and $\overline{RE}$ to logic Low sets RH1782 to half-duplex/loopback mode. In this mode, both the driver and receiver are enabled. The RH1782 is internally connected as half-duplex configuration, such that the non-inverting driver output is connected to the non-inverting receiver input, and the inverting driver output is connected to the inverting receiver input. A logic High at DI input gives a logic High at RO output, and vice versa.

7.1.4 Shutdown mode

Connect DE to logic Low and $\overline{RE}$ to logic High sets RH1782 to shutdown mode. In this mode, both the driver and receiver are disabled. The driver outputs become high impedance, and since RH1782 is internally connected in half-duplex configuration, both A and B pins are resistively connected to ground through the internal receiver input resistors. The receiver output becomes high impedance. In this mode, the RH1782 has the lowest supply current < 1μA.

7.2 Integrated Protection

7.2.1 Bus Fault Protection

The RH1782 features ±70V of fault protection at bus pins. The bus pins A and B can tolerate an external short to fault voltage of -70V to +70V without any damage to the device. Data transmission resumes once the fault voltage is no longer present.

7.2.2 Driver Output Protection

The RH1782 protects the driver output stage against short-circuit to a positive or negative voltage by limiting the output source or sink current. On-chip thermal shutdown circuit further protects the device and disables the driver if the junction temperature of RH1782 exceeds the thermal shutdown threshold.

7.2.3 Driver balanced bus outputs

The RH1782 features high speed balanced driver bus outputs, which minimize EMI and reduce reflections caused by improperly terminated cables. To minimize reflections, the bus lines should be terminated at both cable ends and the termination resistors should match with its cable characteristic impedance, and the stub lengths off the main bus line should be kept as short as possible.

7.2.4 Receiver Failsafe

The RH1782 provides an internal biasing of the receiver input thresholds of ~ -100mV and an input-threshold hysteresis of ~ 30mV such that the receiver output remains at logic High under open bus (both A & B are left open), bus-short (both A and B are shorted together) and idle bus conditions. This failsafe protection provides a known receiver output state when a valid signal is not present at bus lines and prevents the receiver from passing on bus input noise.

7.2.5 Internal Biasing of DI, DE, and $\overline{RE}$ Input Pins

Input pin DI has an internal pull-up to V_{CC}, such that when DI is left floating, the driver outputs are in known states, and when the RH1782 is in loopback mode, the receiver output becomes at logic High, which is a failsafe state. Input pin DE has an internal pull-down to Ground, such that when DE is left floating, the driver is disabled and the power consumption of RH1782 is minimized. Input pin $\overline{RE}$ has an internal pull-up to V_{CC}, such that when $\overline{RE}$ is left floating, the receiver is disabled and the power consumption of RH1782 is minimized.

7.2.6 Under-voltage Detection on Power V_{CC} Pin

The RH1782 incorporates under-voltage detection for V_{CC} pin. The V_{CC} pin supplies power to the device, and if it drops below V_{CC}'s under-voltage threshold, both the driver and receiver will be disabled and the device enters into shutdown mode until V_{CC} has recovered, regardless to the logic state of DE/$\overline{RE}$ pins.

7.2.7 Extended Receiver Input Common-mode Range

The RH1782 features a differential receiver that has an extended input common-mode range from -40V to +40V, exceeding the ANSI TIA/EIA485-A specification of -7V to +12V.It allows an error-free data transmission up to 10Mbps through the whole common-mode range.

7.2.8 ESD Protection

The RH1782 incorporates high ±30kV ESD Human Body Model (HBM) protection at both of the bus A and B pins. In addition, both of the bus pins pass ±8kV IEC Contact Discharge and ±15kV IEC Air Gap Discharge. Furthermore, all pins can tolerate at least ±1.5kV per Charged-device Model (CDM), and pass ±400mA Latch-up (LU) test.

8 Specifications

8.1 Absolute Maximum Ratings

Ratings						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Absolute Maximum Ratings						
V_{CC}	Supply voltage		-0.5		7	V
	Voltage at bus pin - A,B pins		-70		70	V
	Input voltage at any logic pin		-0.3		V_{CC}+0.5	V
	Transient overvoltage pulse through 100Ω per TIA-485		-70		70	V
T_J	Junction temperature				150	°C
T_{stg}	Storage temperature		-55		150	°C
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ESD Ratings						
V_{ESD}	electrostatic discharge voltage	IEC61000-4-2 Contact at bus pins		±8		kV
		IEC61000-4-2 Air Gap at bus pins		±15		kV
		HBM at bus pins		±30		kV
		HBM at other pins		±3		kV
		CDM field induced charge at all pins		±1.5		kV
LU	latch-up	Latch-up test at all pins		±400		mA

8.2 Electrical Characteristics

Electrical Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Recommended Operating Conditions						
V_{CC}	Supply Voltage		3.15	5	5.5	V
V_I	Input voltage at any bus terminal		-40		40	V
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{ID}	Differential input voltage		-7		12	V
I_O	Output current, driver		-60		60	mA
	Output current, receiver		-8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate				10	Mbps
T_A	Operating free-air temperature		-40		125	°C
T_{SD}	Thermal shutdown temperature			160		°C
	Thermal shutdown hystersis			15		°C

V_{CC} = 3.15V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C

Static Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\|V_{OD}\|$	Driver differential output voltage magnitude					
	R_L=60Ω, 4.5V ≤ V_{CC} ≤ 5.5V, 375Ω on each output to -7V to +12V	Figure 4	1.5	2.1		V
	R_L=54Ω, 4.5V ≤ V_{CC} ≤ 5.5V	Figure 3	1.5	2		V
	R_L=54Ω, 3.15V ≤ V_{CC} ≤ 3.45V	Figure 3	0.8	1		V
	R_L=100Ω, 4.5V ≤ V_{CC} ≤ 5.5V	Figure 3	2	2.5		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L=54Ω	-50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Figure 5	1	V_{CC}/2	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage	Figure 5	-50		50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27Ω load resistors, Figure 5		500		mV
C_{OD}	Differential output capacitance			25		pF
V_{IT+}	Positive-going receiver differential input voltage threshold			-100	-35	mV
V_{IT-}	Negative-going receiver differential input voltage threshold		-200	-150		mV
V_{HYS}	Receiver differential input voltage threshold hysteresis (V_{IT+} - V_{IT-})			50		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = -8mA	2.4	V_{CC}-0.1		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8mA		0.1	0.4	V
$I_{I(LOGIC)}$	Driver input, driver enable, and receiver enable input current			30	50	uA
I_{OZ}	Receiver output high-impedance current	V_O = 0V or V_{CC}, $\overline{RE}$ at V_{CC}	-1		1	uA
I_{OS}	Driver short-circuit output current		-250		250	mA
$I_{I(BUS)}$	Bus input current (disabled driver)					
	V_{CC} = 3.15V to 5.5V, or V_{CC} = 0V; DE at 0V	V_I = 12V		75	100	uA
		V_I = -7V	-60	-40		uA
V_{CM}	Receiver Common-mode voltage range	DE = GND, $\overline{RE}$ = GND, no load	-40		40	V
I_{CC}	Supply current (quiescent)					
	Driver and receiver enabled	DE = V_{CC}, $\overline{RE}$ = GND, no load		4	5	mA
	Driver enabled, receiver disabled	DE = V_{CC}, $\overline{RE}$ = VCC, no load		3	5	mA
	driver disabled, receiver enabled	DE = GND, $\overline{RE}$ = GND, no load		2	4	mA
	Driver and receiver disabled (shutdown mode)	DE = GND, DI = open, $\overline{RE}$ = V_{CC}, no load		0.1	1	uA

V_{CC} = 3.15V to 5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C

Switching Characteristics						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver						
t_r, t_f	Driver differential output rise or fall time	R_L=54Ω, C_L=50pF, Figure 3		10	30	ns
t_{PHL}, t_{PLH}	Driver propagation delay	R_L=54Ω, C_L=50pF, Figure 3		15	50	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$	R_L=54Ω, C_L=50pF, Figure 3		2	10	ns
t_{PHZ}, t_{PLZ}	Driver disable time	Receiver enabled, Figure 6		10	100	ns
		Receiver disabled, Figure 6		10	100	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled, Figure 6		10	100	ns
		Receiver disabled, Figure 6		15	30	us
Receiver						
t_r, t_f	Receiver output rise or fall time	C_L=50pF, Figure 7		30	60	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time	C_L=50pF, Figure 7		150	250	ns
$t_{SK(P)}$	Receiver output pulse skew $\|t_{PHL} - t_{PLH}\|$	C_L=50pF, Figure 7		15	50	ns
t_{PHZ}, t_{PLZ}	Receiver disable time	Driver enabled, Figure 8		15	100	ns
		Driver disabled, Figure 9		30	100	ns
t_{PZH}, t_{PZL}	Receiver enable time	Driver enabled, Figure 8		50	100	ns
		Driver disabled, Figure 9		15	30	us

8.1 Test Setup and Timing Diagrams

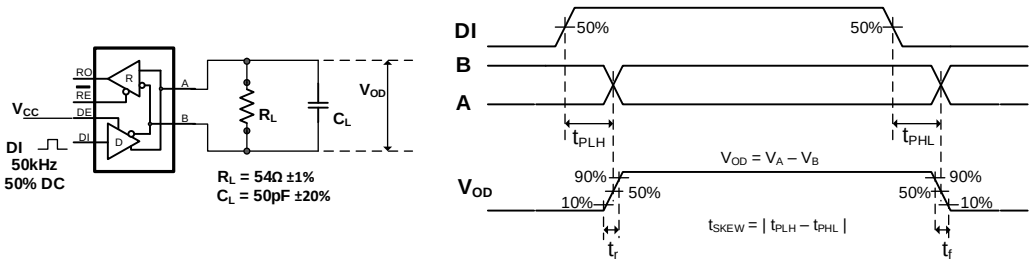


Figure 3 – Driver Differential Output Setup and Timing Diagrams

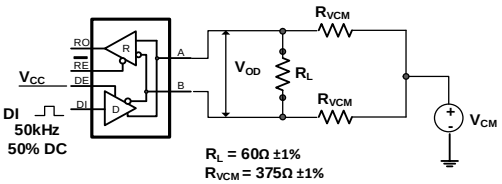


Figure 4 – Driver Differential Output with Common-mode Load Setup

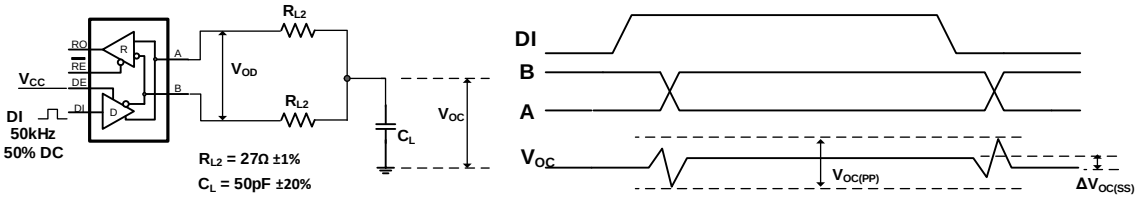
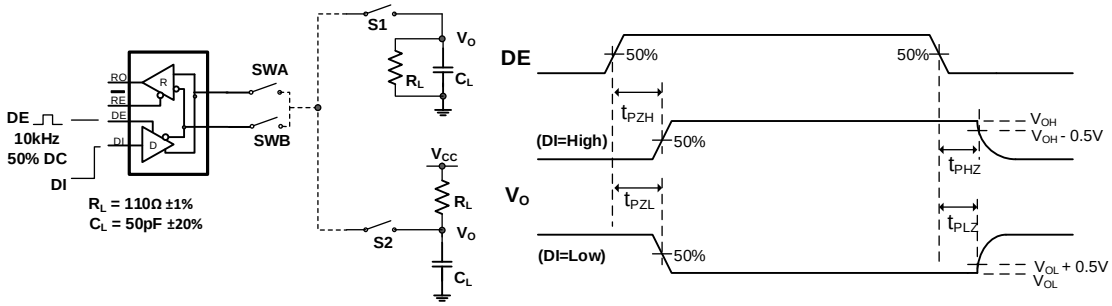


Figure 5 – Driver Differential Common-mode Output with RS-485

Load Setup and Timing Diagrams



Driver	DE	DI	SWA	SWB	S1	S2	Timing
enable	L->H	High	Close	Open	Close	Open	tPZH_A
		Low	Close	Open	Open	Close	tPZL_A
		High	Open	Close	Open	Close	tPZL_B
		Low	Open	Close	Close	Open	tPZH_B
disable	H->L	High	Close	Open	Close	Open	tPHZ_A
		Low	Close	Open	Open	Close	tPLZ_A
		High	Open	Close	Open	Close	tPLZ_B
		Low	Open	Close	Close	Open	tPHZ_B

Figure 6 – Driver Enable and Disable Setup and Timing Diagrams

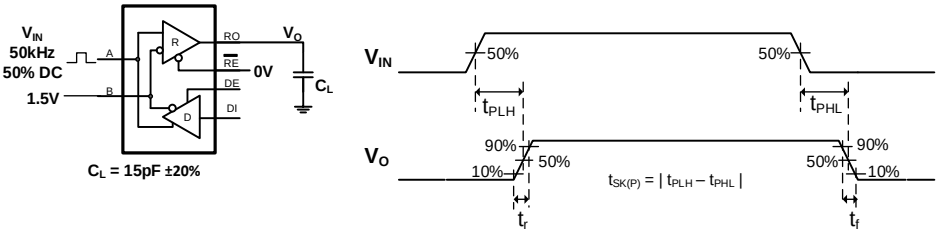
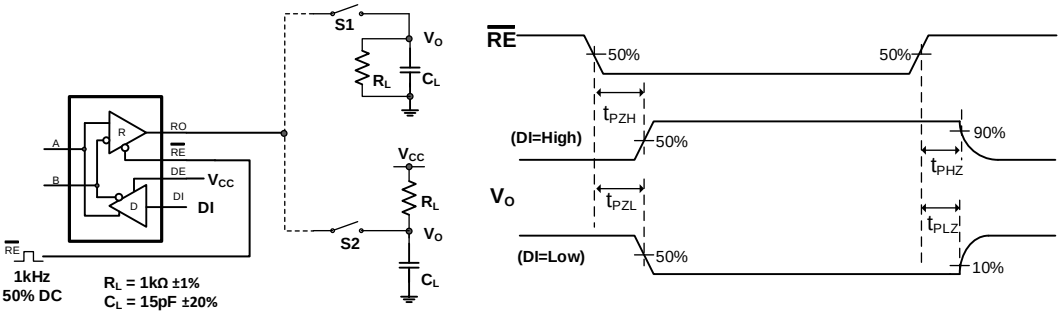
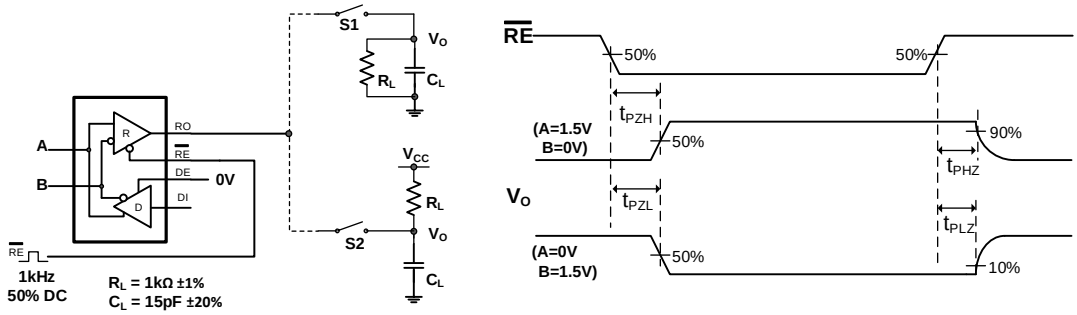


Figure 7 – Receiver Output Setup and Timing Diagrams



Receiver	_RE	DI	SI	S2	Timing
enable	H->L	High	Close	Open	tPZH
		Low	Open	Close	tPZL
disable	L->H	High	Close	Open	tPHZ
		Low	Open	Close	tPLZ

Figure 8 – Receiver Enable and Disable with Driver Enabled Setup and Timing Diagrams

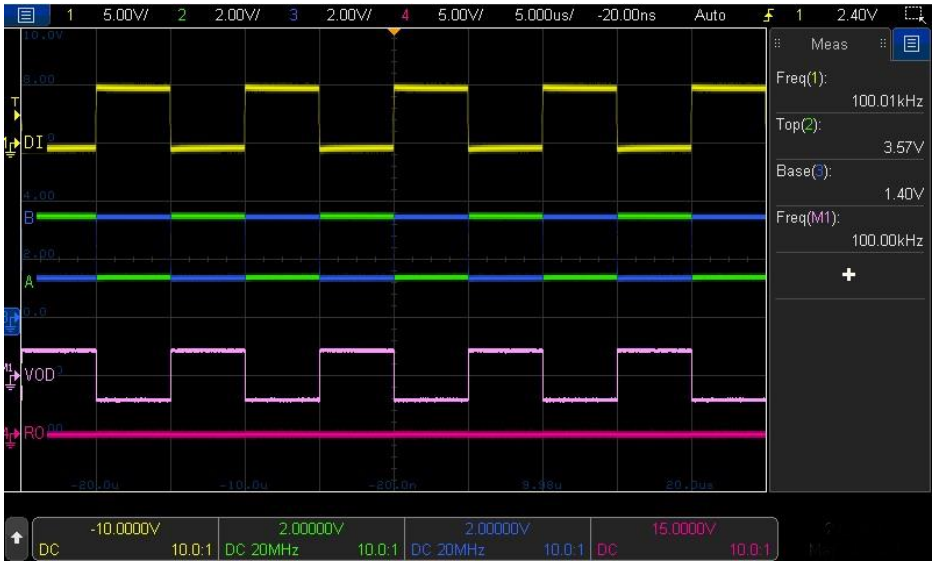


Receiver	_RE	A	B	S1	S2	Timing
enable	H->L	1.5V	0V	Close	Open	tPZH
		0V	1.5V	Open	Close	tPZL
disable	L->H	1.5V	0V	Close	Open	tPHZ
		0V	1.5V	Open	Close	tPLZ

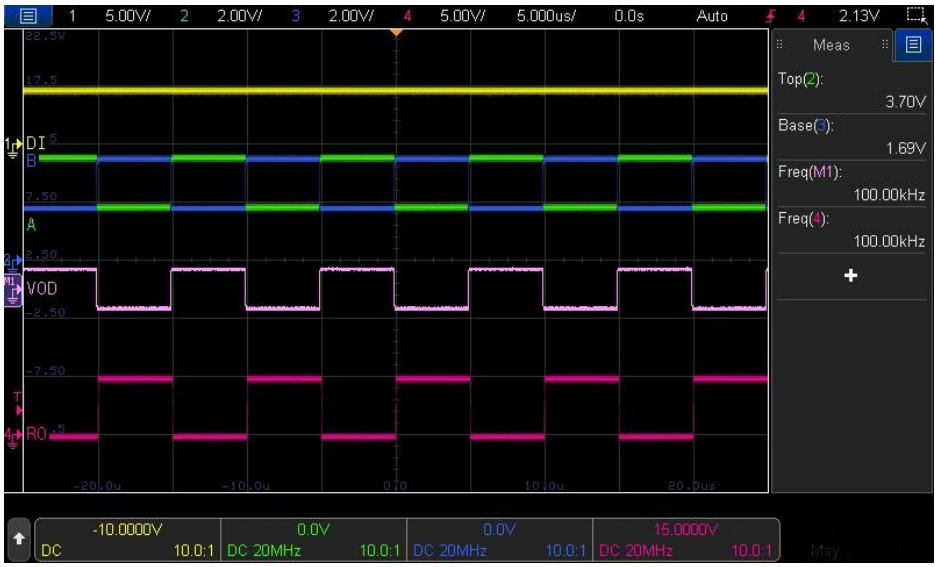
Figure 9 – Receiver Enable and Disable with Driver Disabled Setup and Timing Diagrams

9 Typical Operating Characteristics

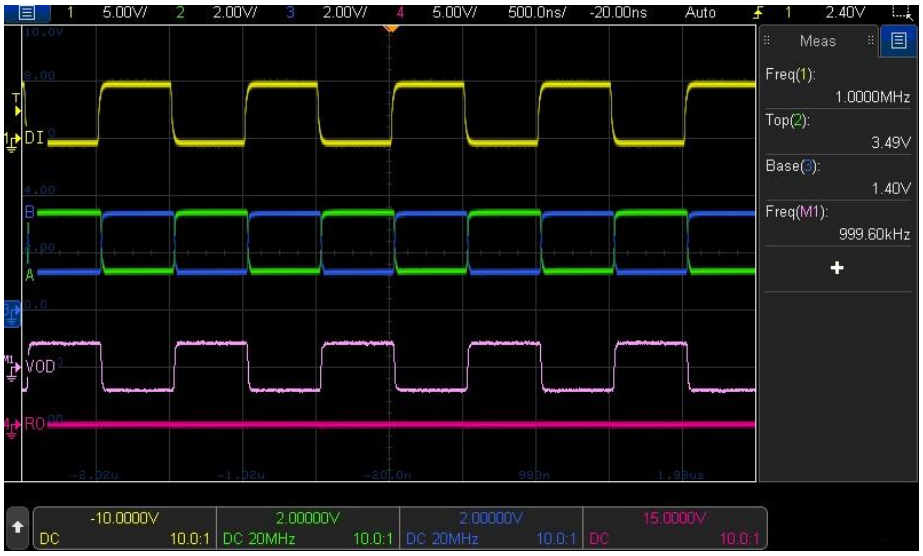
V_{CC}=5.0V, R_L=54Ω, C_L=50pF, T_A=25°C, unless specified otherwise.



200Kbps waveform of Driver mode ($\overline{RE}$= V_{CC}, DE=V_{CC})

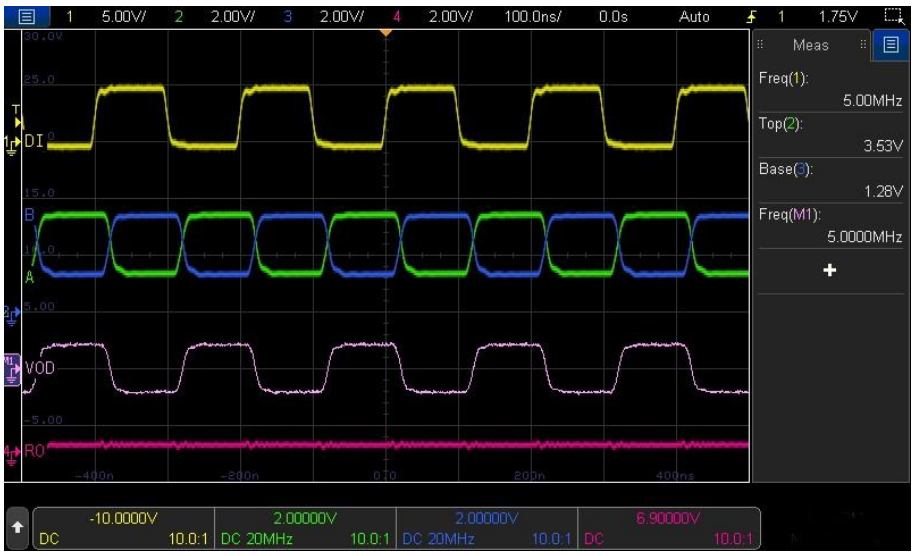


200Kbps waveform of Receiver mode ($\overline{RE}$=GND, DE=GND)

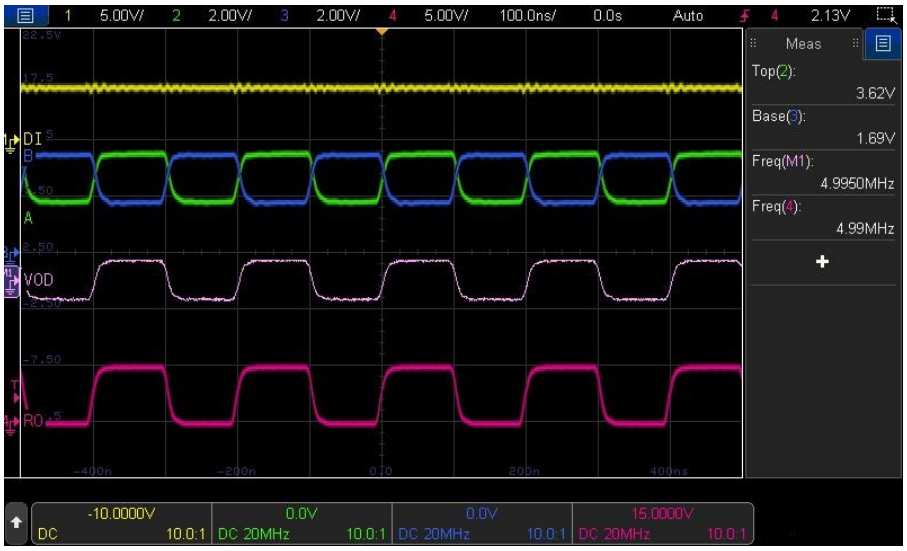


2Mbps waveform of Driver mode ($\overline{RE}$= V_{CC}, DE=V_{CC})

2Mbps waveform of Receiver mode ($\overline{RE}$=GND, DE=GND)



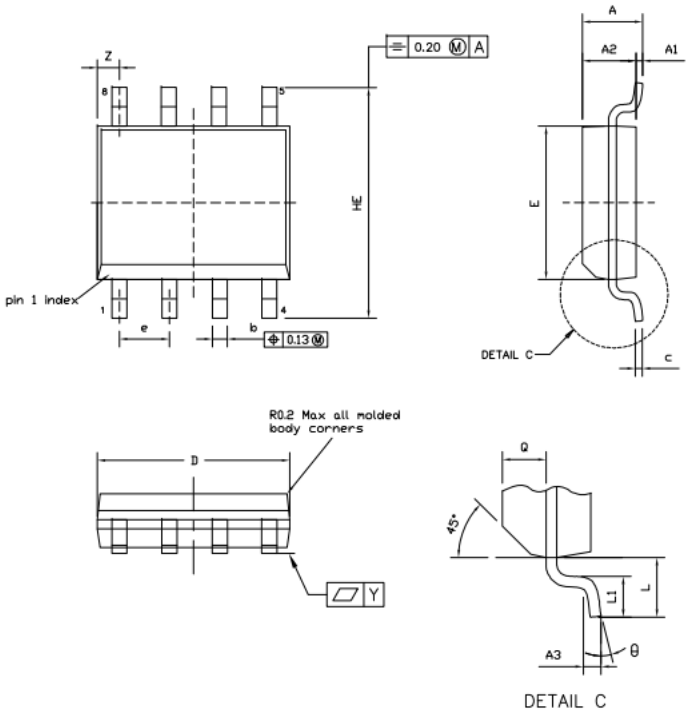
10Mbps waveform of Driver mode ($\overline{RE}$= V_{CC}, DE=V_{CC})



10Mbps waveform of Receiver mode ($\overline{RE}$=GND, DE=GND)

10 Package Information

Package Outline SO-8 (150 mil)



DETAIL C

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°